Insert at page 23, before line 25:

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Figs. 17A-B depict connection methods in accordance with the prior art and the present invention;

In the Claims:

Following is a list of all pending claims.

Marked up versions of all revised claims, showing insertions and deletions, are included in Appendix B.

85. A method of sending data from a first module to a second module in a modular digital system, said method comprising the steps of:

applying signals representative of the data to a first half-capacitor associated with said first module;

capacitively coupling said first half-capacitor to a second half-capacitor, associated with said second module; and,

receiving, at said second module and via said second half-capacitor, a signal related to the signals applied to said first half-capacitor.

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86. (Amended) A method of coupling signals between electronic devices in a modular electronic system, said method comprising the steps of:

locating a first subset of said electronic devices on a first semiconductor chip;

locating a second subset of said electronic devices on a second semiconductor chip; and,

aligning and affixing said first and second chips so as to capacitively couple said first and second chips.

87. A method of coupling signals between electronic devices in a modular electronic system as defined in claim 86 wherein the first and second chips are affixed to a base substrate thereby capacitively coupling said first and second chips via said substrate.

100. (Amended) A method of capacitively coupling signals between first and second semiconductor chips, each said chip having a plurality of half-capacitors, said method comprising the steps of:

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affixing said first chip to a substrate;

aligning said second chip to said first chip; and,

affixing said second chip to said substrate, thereby capacitively coupling corresponding half-capacitors on said first and second chips and providing direct capacitive coupling between said first and second chips.

In the Abstract:

The Abstract was not filed with application. Please insert the following Abstract.

Methods and apparatus are described for capacitively signaling between different semiconductor chips and modules without the use of connectors, solder bumps, wire-bond interconnections or the like. Preferably, pairs of half-capacitor plates, one half located on each chip, module or substrate are used to capacitively couple signals from one chip, module or substrate to another. The use of plates relaxes the need for high precision alignment as well as reduces the area needed to effect signaling, and reduces or eliminates the requirements for exotic metallurgy.

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